## Search Results

Search Results for: **[(instruction <NEAR/2> preload*)]**
Found **12** of **127,132 searched.**

### Search within Results



**Results 1 - 12 of 12** short listing

**1** Tiny instruction caches for low power embedded systems 100%
Ann Gordon-Ross , Susan Cotterell , Frank Vahid
**ACM Transactions on Embedded Computing Systems (TECS)** November 2003
Volume 2 Issue 4
Instruction caches have traditionally been used to improve software performance. Recently, several tiny instruction cache designs, including filter caches and dynamic loop caches, have been proposed to instead reduce software power. We propose several new tiny instruction cache designs, including preloaded loop caches, and one-level and two-level hybrid dynamic/preloaded loop caches. We evaluate the existing and proposed designs on embedded system software benchmarks from both the Powerstone and ...

**2** Hardware implementation of loop trace and microprogram synthesis 100%
A. M. ADB-Alla , Laird H. Moffett
**Proceedings of the 1975 annual conference** January 1975
The modification or tuning of the microcode in a computer that utilizes a writable control store is one method whereby a program's execution time can be improved. A method for automatically performing a microcode tuning or synthesis has been developed by Drs. Karlgaard and Abd-alla and is discussed in detail in [1]. Presented is an extension of this effort which allows microcode synthesis to be performed "on-the-fly". This is accomplished by: (1) performing the required program ...

**3** On-line architecture tuning using microcapture 100%
A. M. Abd-Alla , Laird H. Moffett
**ACM SIGARCH Computer Architecture News , Proceedings of the 3rd annual symposium on Computer architecture** January 1976
Volume 4 Issue 4

## Search Results

Search Results for: **[(prefix <NEAR/2> buffer*)]**
Found **7** of **127,132 searched.**

### Search within Results



**Results 1 - 7 of 7** short listing

**1** Session 6: Log write-ahead protocols and IMS/VS logging 100%
R. J. Peterson , J. P. Strickland
**Proceedings of the 2nd ACM SIGACT-SIGMOD symposium on Principles of database systems** March 1983

**2** Purely functional, real-time deques with catenation 100%
Haim Kaplan , Robert E. Tarjan
**Journal of the ACM (JACM)** September 1999
Volume 46 Issue 5
We describe an efficient, purely functional implementation of deques with catenation. In addition to being an intriguing problem in its own right, finding a purely functional implementation of catenable deques is required to add certain sophisticated programming constructs to functional programming languages. Our solution has a worst-case running time of O(1) for each push, pop, inject, eject and catenation. The best previously known solution has an O(log

**3** Literate programming 100%
Christopher J. Van Wyk
**Communications of the ACM** December 1988
Volume 31 Issue 12

**4** An introduction to assertional reasoning for concurrent systems 100%
A. Udaya Shankar
**ACM Computing Surveys (CSUR)** September 1993
Volume 25 Issue 3
This is a tutorial introduction to assertional reasoning based on temporal logic. The

## Search Results

Search Results for: **[(prefix <NEAR/2> cach*)]**
Found **32** of **127,132 searched.**

### Search within Results

> Advanced Search

> Search Help/Tips

**Sort by:** Title Publication Publication Date **Score** Binder

**Results 1 - 20 of 32** short listing

Prev Page 1 2 Next Page

**1** Segment-based proxy caching of multimedia streams 100%
Kun-Lung Wu , Philip S. Yu , Joel L. Wolf
**Proceedings of the tenth international conference on World Wide Web** April 2001

**2** Proxy-assisted techniques for delivering continuous multimedia streams 100%
Lixin Gao , Zhi-Li Zhang , Don Towsley
**IEEE/ACM Transactions on Networking (TON)** December 2003
Volume 11 Issue 6
We present a proxy-assisted video delivery architecture that can simultaneously reduce the resources requirements at the central server and the service latency experienced by clients (i.e., end users). Under the proposed video delivery architecture, we develop and analyze two novel proxy-assisted video streaming techniques for on-demand delivery of video objects to a large number of clients. By taking advantage of the resources available at the proxy servers, these techniques not only significan ...

**3** IPStash: a Power-Efficient Memory Architecture for IP-lookup 100%
Stefanos Kaxiras , Georgios Keramidas
**Proceedings of the 36th Annual IEEE/ACM International Symposium on Microarchitecture** December 2003
High-speed routers often use commodity, fully-associative,TCAMs (Ternary Content AddressableMemories) to perform packet classification and routing(IP-lookup). We propose a memory architecture calledIPStash to actasa TCAMreplacement,offering

## Search Results

Search Results for: **[(cacheless OR cache-less)]**
Found **49** of **127,132 searched.**

### Search within Results

> Advanced Search

> Search Help/Tips

**Sort by:** Title Publication Publication Date **Score** Binder

**Results 1 - 20 of 49** short listing

Prev Page 1 2 3 Next Page

**1** Performance issues of enterprise level web proxies 99%

Carlos Maltzahn , Kathy J. Richardson , Dirk Grunwald

**ACM SIGMETRICS Performance Evaluation Review , Proceedings of the 1997 ACM SIGMETRICS international conference on Measurement and modeling of computer systems** June 1997

Volume 25 Issue 1

Enterprise level web proxies relay world-wide web traffic between private networks and the Internet. They improve security, save network bandwidth, and reduce network latency. While the performance of web proxies has been analyzed based on synthetic workloads, little is known about their performance on real workloads. In this paper we present a study of two web proxies (CERN and Squid) executing real workloads on Digital's Palo Alto Gateway. We demonstrate that the simple CERN proxy architecture ...

**2** Session 9: hardware performance: Cache performance in vector supercomputers 91%

L. I. Kontothanassis , R. A. Sugumar , G. J. Faanes , J. E. Smith , M. L. Scott

**Proceedings of the 1994 ACM/IEEE conference on Supercomputing** November 1994

Traditional supercomputers use a flat multi-bank SRAM memory organization to supply high bandwidth at low latency. Most other computers use a hierarchical organization with a small SRAM cache and slower, cheaper DRAM for main memory. Such systems rely heavily on data locality for achieving optimum performance. This paper evaluates cache-based memory systems for vector supercomputers. We develop a simulation model for a cache-based version of the Cray Research C90 and use the NAS parallel

## Search Results

Search Results for: **["real-time" <NEAR/4> (cache OR buffer)]**
Found **173** of **127,132 searched.**

### Search within Results

> Advanced Search

> Search Help/Tips

**Sort by:** Title Publication Publication Date Score Binder

**Results 1 - 20 of 173** short listing

Prev Page 1 2 3 4 5 6 7 8 9 Next Page

**1** Low power signal processing architectures for network microsensors 100%
Michael J. Dong , K. Geoffrey Yung , Wiliam J. Kaiser
**Proceedings of the 1997 international symposium on Low power electronics and design** August 1997

**2** Novel ideas: Using variable-MHz microprocessors to efficiently handle uncertainty in real-time systems 100%
Eric Rotenberg
**Proceedings of the 34th annual ACM/IEEE international symposium on Microarchitecture** December 2001
Guaranteed performance is critical in real-time systems because correct operation requires tasks complete on time. Meanwhile, as software complexity increases and deadlines tighten, embedded processors inherit high-performance techniques such as pipelining, caches, and branch prediction. Guaranteeing the performance of complex pipelines is difficult and worst-case analysis often under-estimates the microarchitecture for correctness. Ultimately, the designer must turn to clock frequency as a reli ...

**3** Virtual simple architecture (VISA): exceeding the complexity limit in safe real-time systems 100%
Aravindh Anantaraman , Kiran Seth , Kaustubh Patil , Eric Rotenberg , Frank Mueller
**ACM SIGARCH Computer Architecture News , Proceedings of the 30th annual international symposium on Computer architecture** May 2003
Volume 31 Issue 2

Your search matched **277** of **1006282** documents.
A maximum of **500** results are displayed, **15** to a page, sorted by **Relevance Descending** order.

**Refine This Search:**
You may refine your search by editing the current search expression or enter new one in the text box.

(real time) <and> cache Search

☐ Check to search within this result set

**Results Key:**
**JNL** = Journal or Magazine **CNF** = Conference **STD** = Standard

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1 **Performance tradeoffs in real-time transaction processing with clie data caching**
*Hyunchul Kang; YoungSung Kim;*
Database Engineering and Applications, 1999. IDEAS '99. International Symp Proceedings , 2-4 Aug. 1999
Pages:403 - 407

[Abstract] [PDF Full-Text (72 KB)] **IEEE CNF**

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2 **Low-complexity algorithms for static cache locking in multitasking real-time systems**
*Puaut, I.; Decotigny, D.;*
Real-Time Systems Symposium, 2002. RTSS 2002. 23rd IEEE , 3-5 Dec. 200
Pages:114 - 123

[Abstract] [PDF Full-Text (376 KB)] **IEEE CNF**

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3 **On predictability and optimization of multiprogrammed caches for r time applications**
*Shahrier, S.M.; Juh-Charn Liu;*
Performance, Computing, and Communications Conference, 1997. IPCCC 199 IEEE International , 5-7 Feb. 1997
Pages:17 - 25

[Abstract] [PDF Full-Text (796 KB)] **IEEE CNF**

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4 **OS-controlled cache predictability for real-time systems**

Your search matched **6** of **1006282** documents.
A maximum of **500** results are displayed, **15** to a page, sorted by **Relevance Descending** order.

**Refine This Search:**
You may refine your search by editing the current search expression or enter new one in the text box.

cacheless <or> cache less Search

☐ Check to search within this result set

**Results Key:**
**JNL** = Journal or Magazine **CNF** = Conference **STD** = Standard

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1 **Set-associative dynamic random access memory**
*Ward, S.A.; Zak, R.C.;*
Computer Design: VLSI in Computers and Processors, 1988. ICCD '88., Proceedings of the 1988 IEEE International Conference on , 3-5 Oct. 1988
Pages:478 - 483

[Abstract] [PDF Full-Text (412 KB)] **IEEE CNF**

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2 **MACS: a predictable architecture for real time systems**
*Cogswell, B.; Segall, Z.;*
Real-Time Systems Symposium, 1991. Proceedings., Twelfth , 4-6 Dec. 1991
Pages:296 - 305

[Abstract] [PDF Full-Text (752 KB)] **IEEE CNF**

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3 **Improving memory energy using access pattern classification**
*Kandemir, M.; Sezer, U.; Delaluz, V.;*
Computer Aided Design, 2001. ICCAD 2001. IEEE/ACM International Conferei on , 4-8 Nov. 2001
Pages:201 - 206

[Abstract] [PDF Full-Text (602 KB)] **IEEE CNF**

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4 **Cache performance in vector supercomputers**
*Kontothanassis, L.I.; Sugumar, R.A.; Faanes, G.J.; Smith, J.E.; Scott, M.L.;*
Supercomputing '94. Proceedings , 14-18 Nov. 1994
Pages:255 - 264

Your search matched **13** of **1006282** documents.
A maximum of **500** results are displayed, **15** to a page, sorted by **Relevance Descending** order.

**Refine This Search:**
You may refine your search by editing the current search expression or enter new one in the text box.

prefix <near/2> cache Search

☐ Check to search within this result set

**Results Key:**
**JNL** = Journal or Magazine **CNF** = Conference **STD** = Standard

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1 **Batched patch caching for streaming media**
*Frossard, P.; Verscheure, O.;*
Communications Letters, IEEE , Volume: 6 , Issue: 4 , April 2002
Pages:159 - 161

[Abstract] [PDF Full-Text (211 KB)] **IEEE JNL**

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2 **Protocol considerations for video prefix-caching proxy in wide area networks**
*Hyotaek Lim; Du, D.H.C.;*
Electronics Letters , Volume: 37 , Issue: 6 , 15 Mar 2001
Pages:403 - 404

[Abstract] [PDF Full-Text (216 KB)] **IEE JNL**

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3 **Multilevel aligned IP prefix caching based on singleton information**
*Woei-Luen Shyu; Cheng-Shong Wu; Ting-Chao Hou;*
Global Telecommunications Conference, 2002. GLOBECOM '02. IEEE , Volume 3 , 17-21 Nov. 2002
Pages:2345 - 2349 vol.3

[Abstract] [PDF Full-Text (489 KB)] **IEEE CNF**

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4 **Reducing cache miss ratio for routing prefix cache**
*Huan Liu;*
Global Telecommunications Conference, 2002. GLOBECOM '02. IEEE , Volume 3 , 17-21 Nov. 2002

Your search matched **0** of **1006282** documents.
A maximum of **500** results are displayed, **15** to a page, sorted by **Relevance Descending** order.

**Refine This Search:**
You may refine your search by editing the current search expression or enter new one in the text box.

prefix <near/2> buffer Search

☐ Check to search within this result set

**Results Key:**
**JNL** = Journal or Magazine **CNF** = Conference **STD** = Standard

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**Results:**
**No documents matched your query.**